

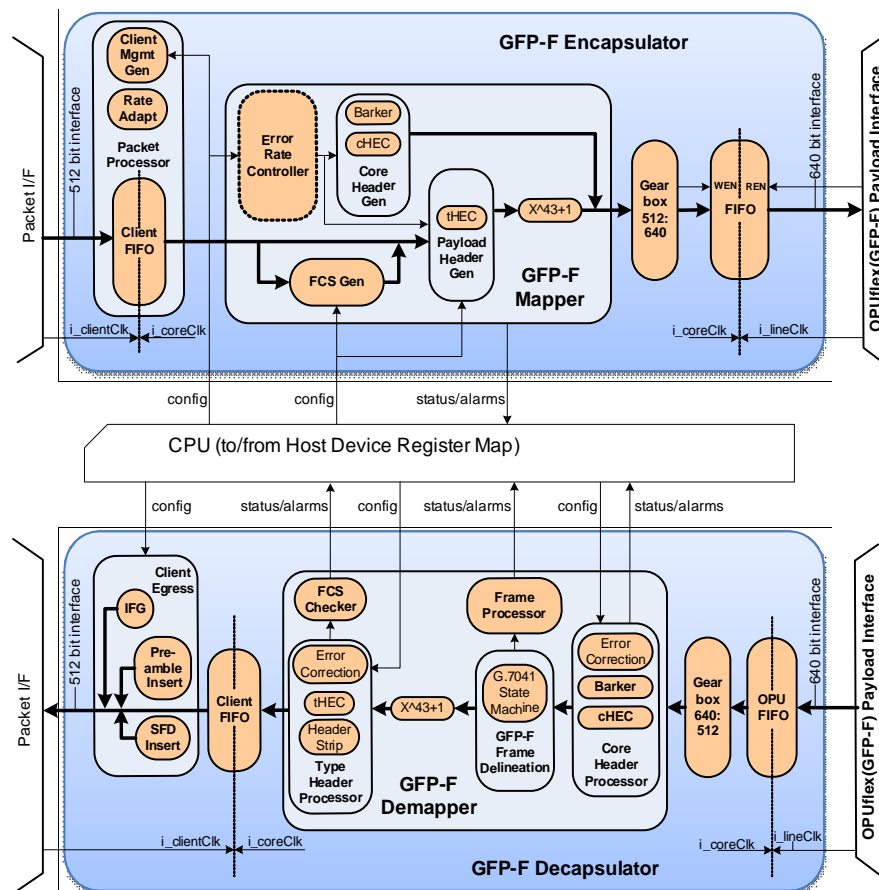
100G GFP-F Mapper Core

Sembarc's flexible 100G GFP-F Mapper IP core (SKC5002) is capable of processing multi-rate Ethernet clients from 1Gbps to 100Gbps. This IP core is a standalone component within Sembarc's family of 100G capable FEC and OTN IP cores and solutions.

Overview

The SKC5002 core is a single channel, ultra-compact 100G GFP-F IP core for encapsulating and decapsulating Ethernet MAC frames at rates of 1Gbps up to 100Gbps in compliance with ITU-T G.7041 and ITU-T G.709 17.4.

Block Diagram



General Features

- 100G throughput
- Suitable for FPGA and ASIC
- ITU-T G.7041/Y.1303 compliant
- Supports data client interfaces from 1GbE to 100GbE
- Supports client data, control and client management frames
- Extensive alarm support
- GFP-F performance monitoring
- Transparent Preamble and SFD

Encapsulator

- GFP frame mapping as per G.7041 section 7.1
- User configurable scrambling of the GFP core header and payload
- User config. GFP FCS insertion
- Core and Type header support for bit error detection/correction
- Rate adaptation support via GFP idle frames
- Supports Jumbo frames

Decapsulator

- Performs GFP frame delineation as per G.7041 section 6.3.1
- Support for single bit error correction of core & type header
- User configurable descrambling
- Support for pFCS verification
- Support for frame-discard for 'too short' and 'too long' packets

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Resources	LUTs	FFs	Memory
Encapsulator	38.5 k	23.8 k	431.8 kbit
Decapsulator	52.0 k	43.4 k	252.2 kbit
Total (1)	90.5k	74.6 k	684 kbit
Fmax (2)	>210MHz		

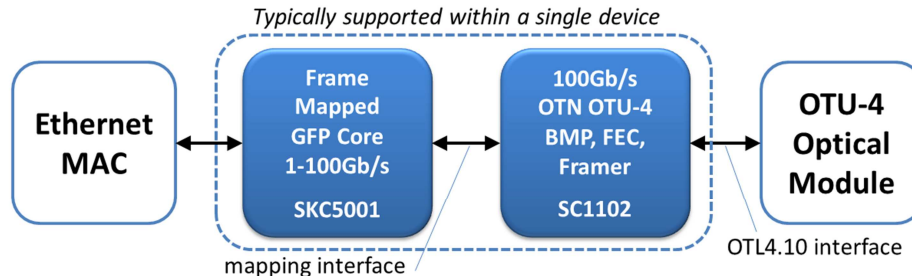
- (1) Resource figures are provided as a guideline only and architecture specific. Sembarc will support customisation requests which may affect utilisation figures. Memory figures are device dependent; with some architectures logic can be traded for memory resource. Sizes shown are for part# SKC5002A (see 'Part Numbers' below).
- (2) Performance figure is provided as a guideline only and is based on the fastest Speed Grade of the highest performing devices. Figure may be less for slower performing devices.

Deliverables	
IP Core format	EDIF file
Simulation	Encrypted Modelsim Back annotated VHDL.
Constraints	Format as required
Verification	Verilog / PLI testsuite
Documentation	Datasheet (available)

Typical Applications

- OTN/SONET add/drop multiplexers
- Optical/Digital switch interfacing
- OTN Data Fabric interfacing (via SAR)
- OTN and/or SONET/SDH line cards
- Test equipment (SKC5002 is tailored for use within test equipment, see 'Part Numbers' section below)

Application Example



The application shown involves the mapping of Ethernet packets into GFP for transport within the payload of a 100Gbps digital wrapper framer core. This can be achieved by using the SKC5002/1 core in conjunction with Sembarc's SC1102 OTN FEC/Framer IP core (variants available - contact us for details).

Part Numbers

Sembarc's flexible 100G GFP-F Mapper IP is currently available in two versions

- **SKC5002A**- GFP-F core with error insertion capability, suitable for use within test equipment
- **SKC5001A**- GFP-F core optimised for size, and without error insertion capability

Sembarc End-to-End Design Services

To complement our IP offerings Sembarc offers a full range of design services to help reduce the development cycle of complex FPGA designs. These services include: System Architecture, Requirements Capture, Detailed Design, IP Integration, Maintenance, and Device Verification.

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